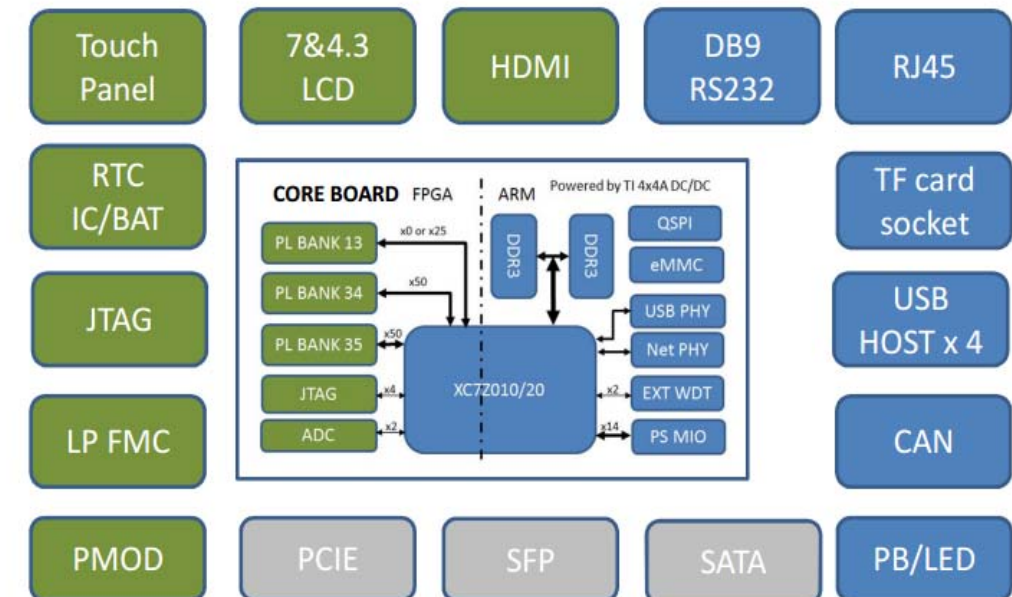


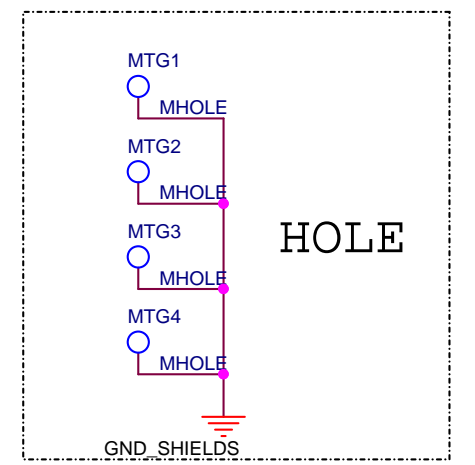
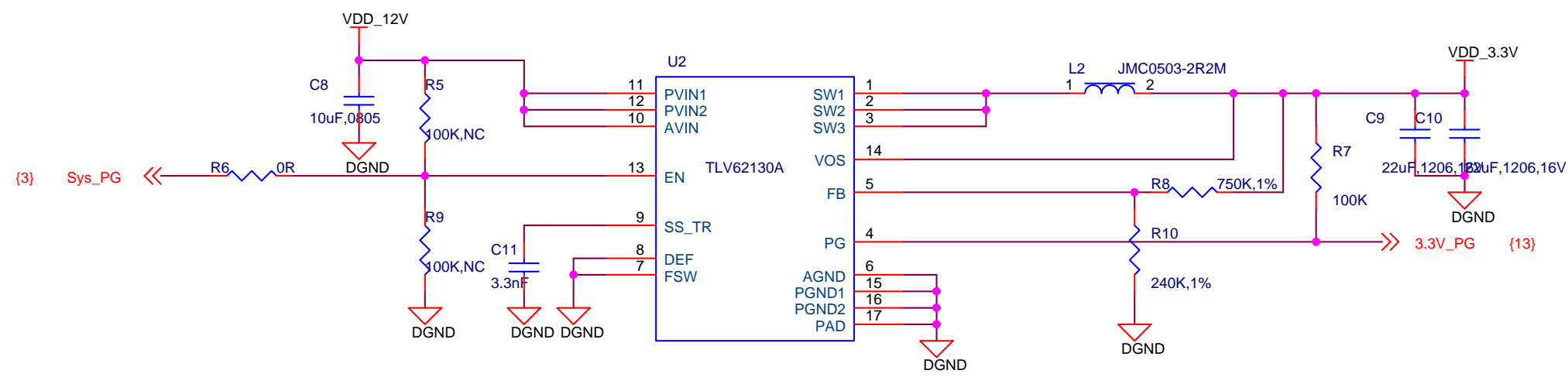
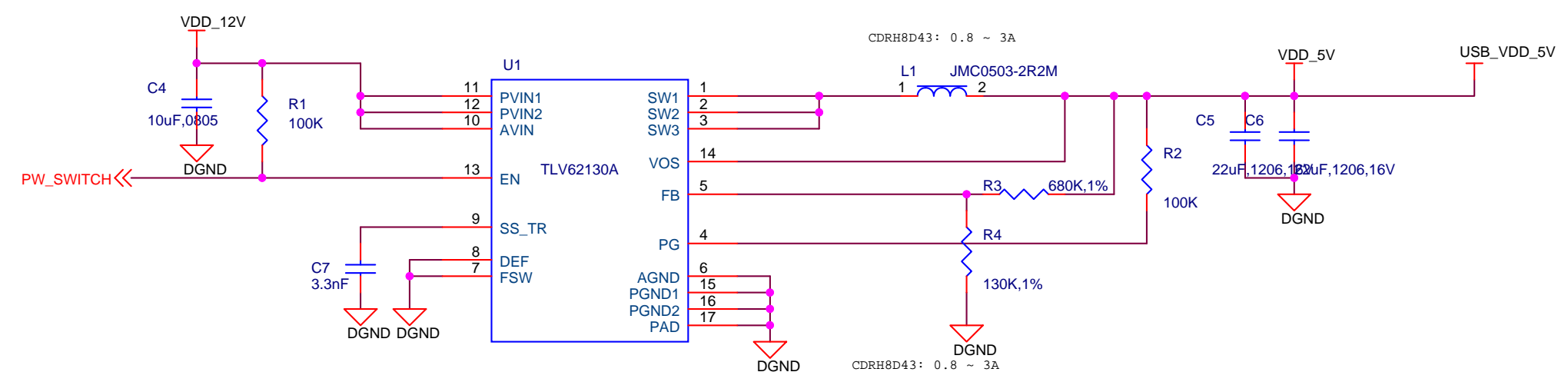
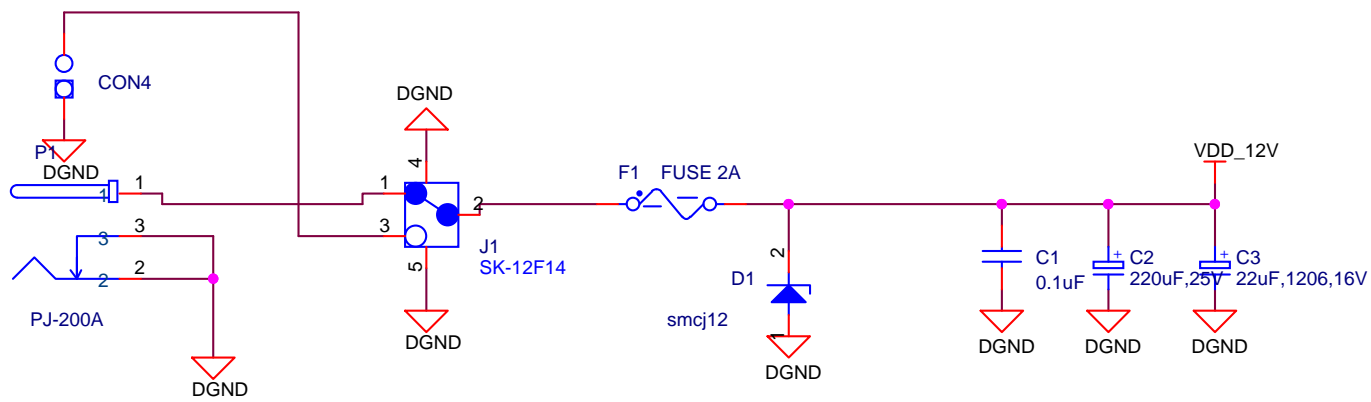
REV	Description	DATE	BY
Ver 1	Initial Release.	2015-03-25	M
Ver 1.1	Modify Jtag, SN74AUP2G08 Package; Seperate PENINQ and TPINT; ADD R185 10K;U29; Update value	2015-05-11	M

PAGE NO.	SCHEMATIC PAGE
1	TITLE PAGE
2	POWER
3	Exp Conn
4	USB HOSTx4
5	DEBUG_RS232_JTAG
6	PHY_NET1
7	HDMI
8	LCD
9	PMOD & CAN & LVDS PAIRS
10	PCIE
11	SFP & SATA
12	LP FMC
13	MISC

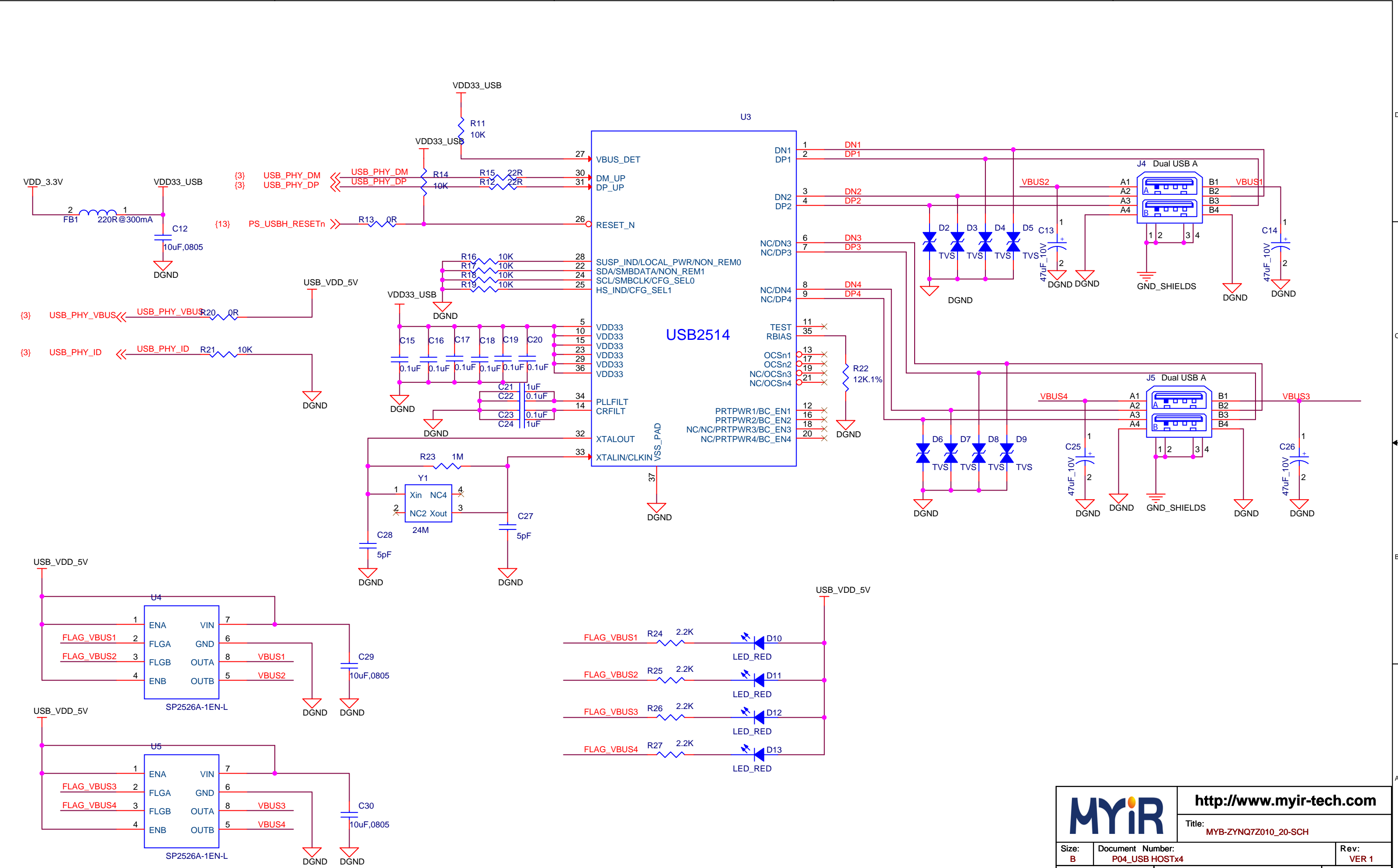
## Zynq 7000 DevKit


- : FPGA RESOURCE
- : ARM RESOURCE
- : ONLY FOR 7015

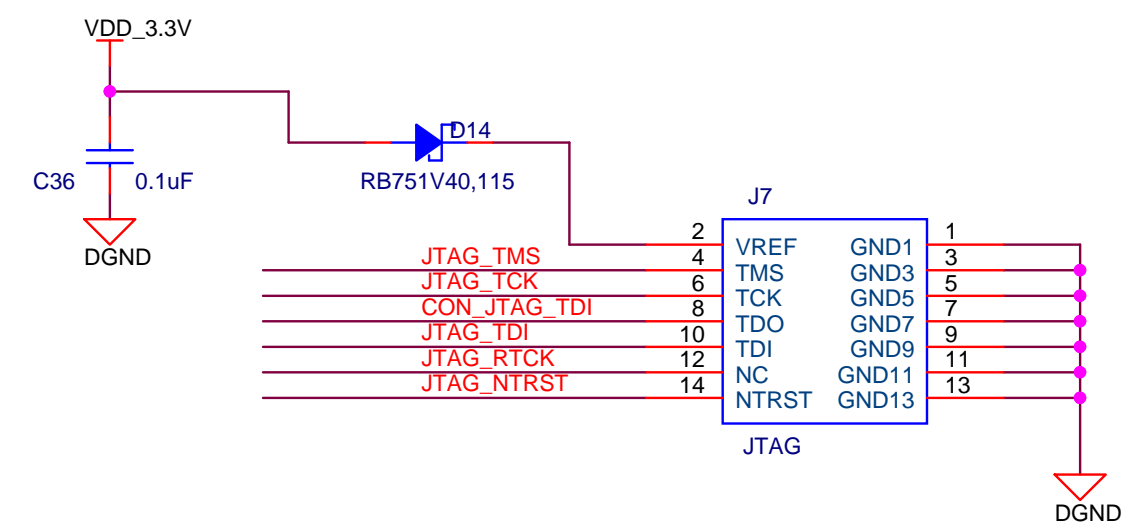
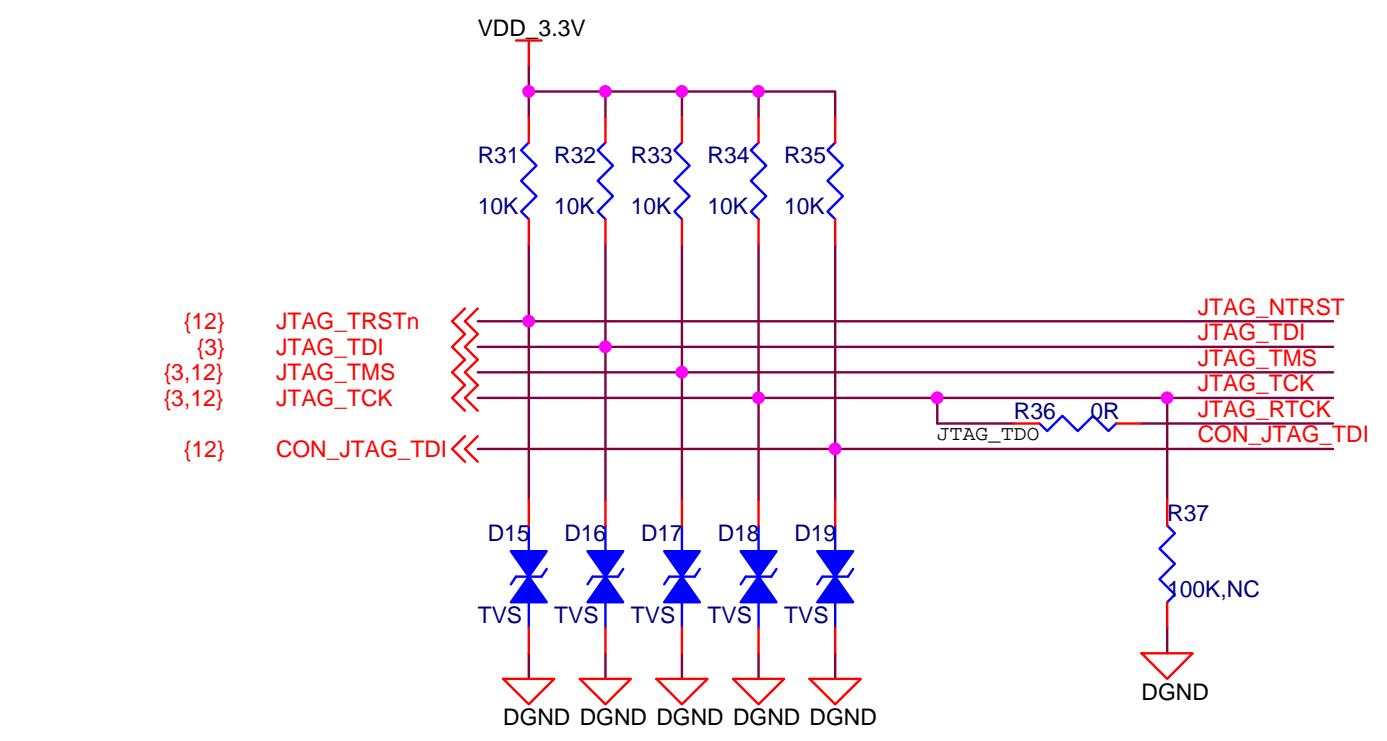
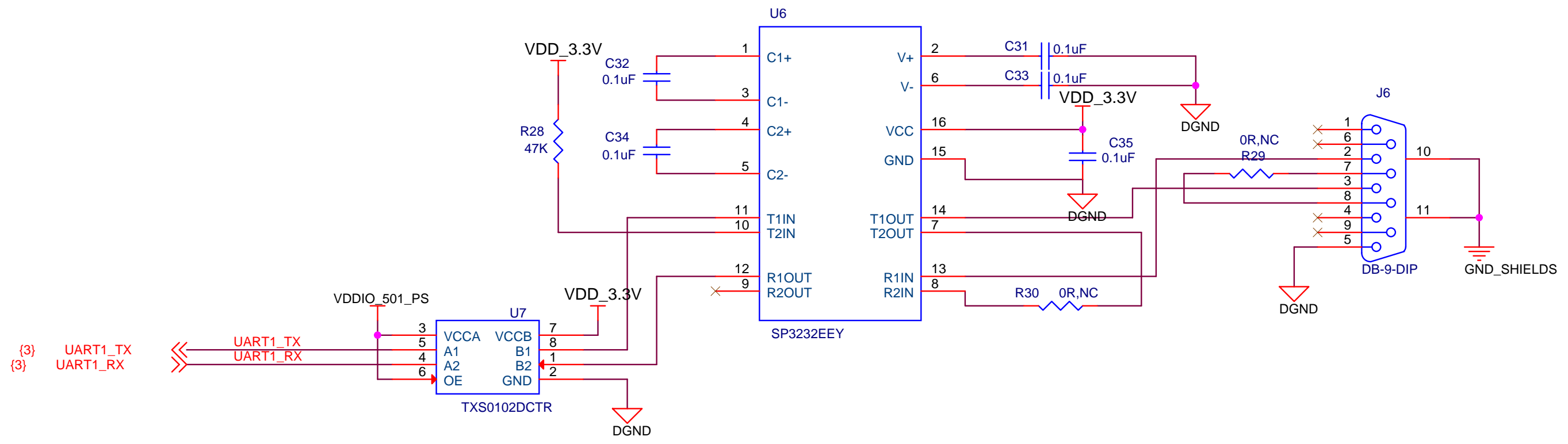





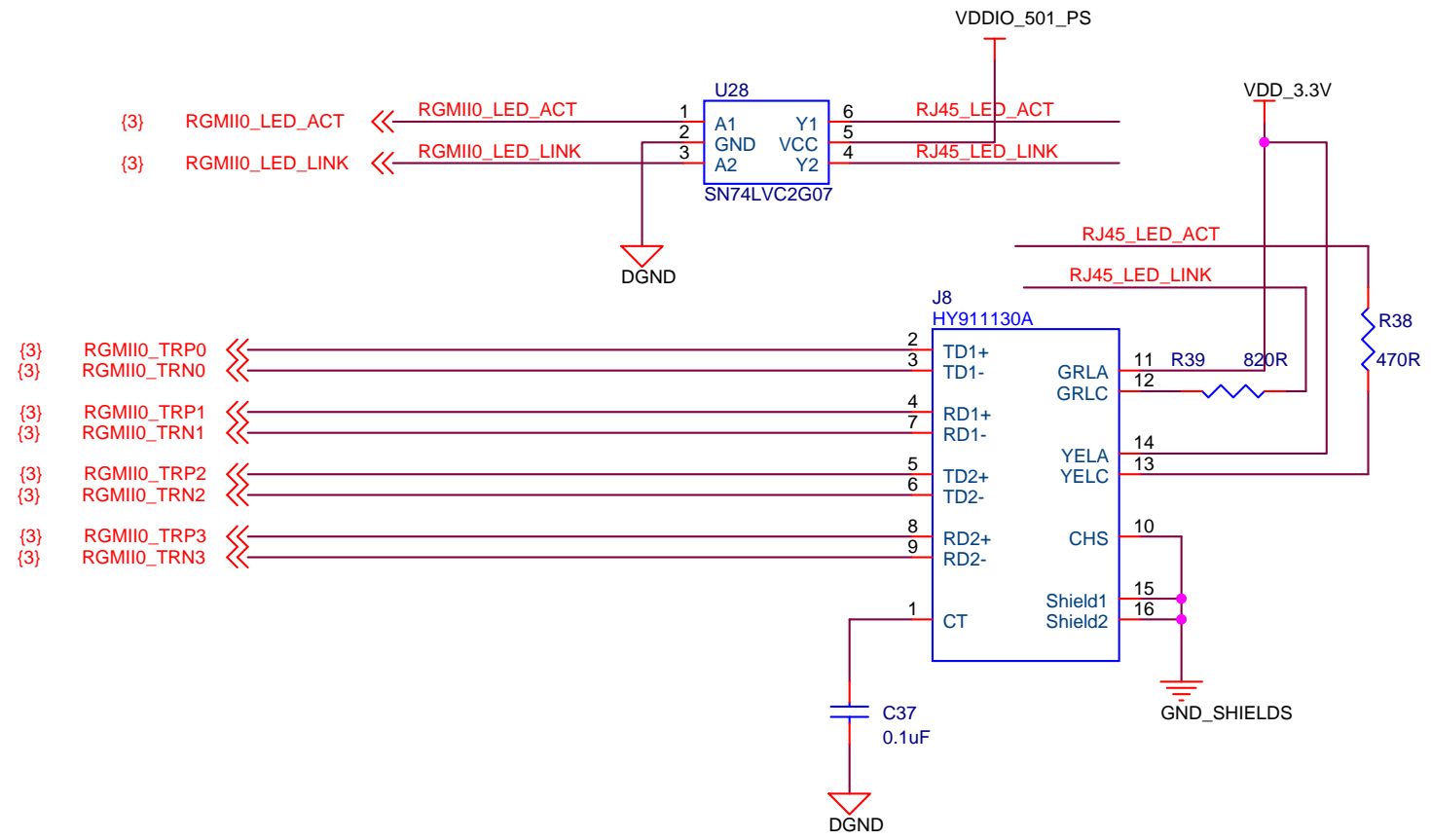




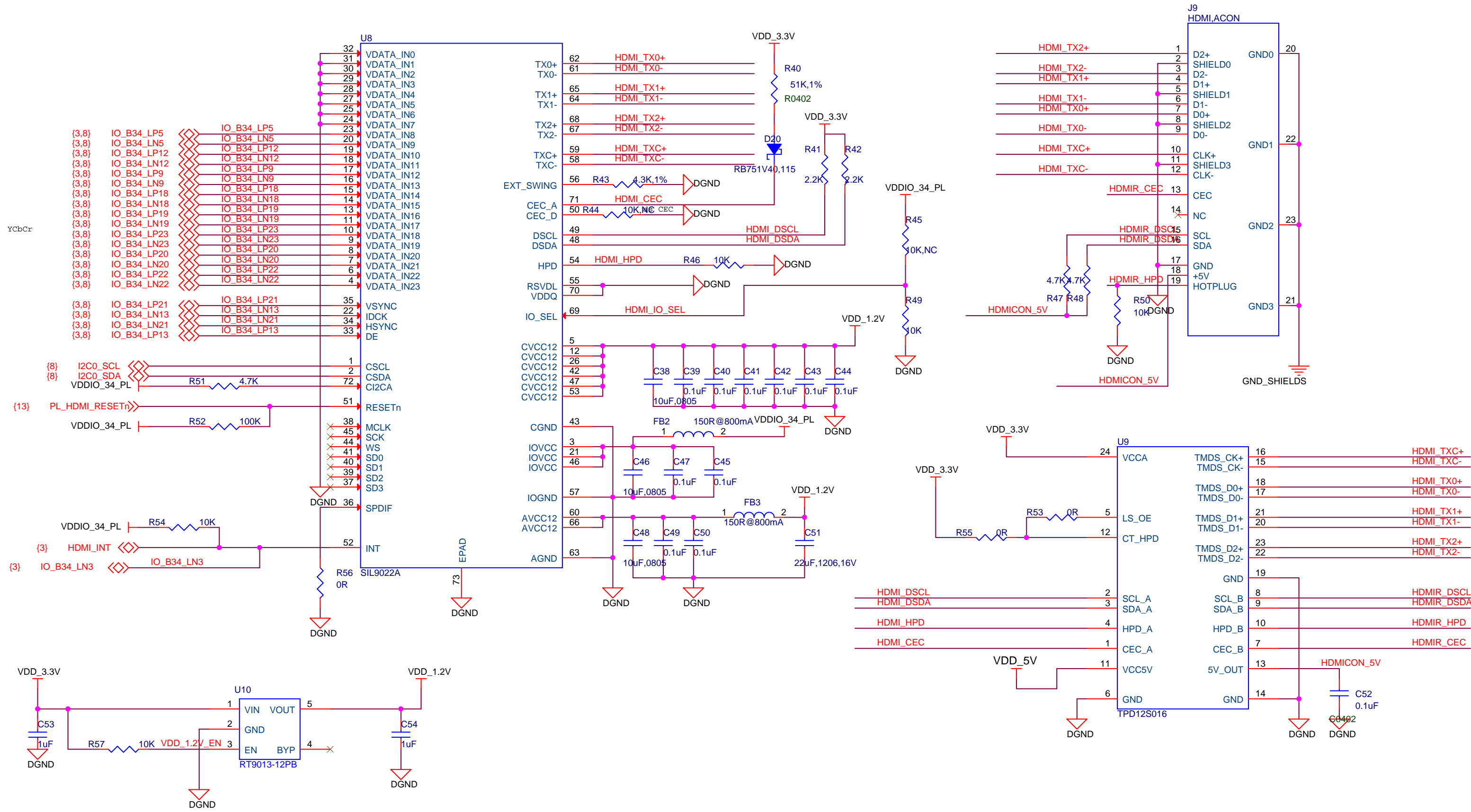
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Draw By: MYIR	Date: Thursday, July 13, 2017	Sheet: 4 of 13	

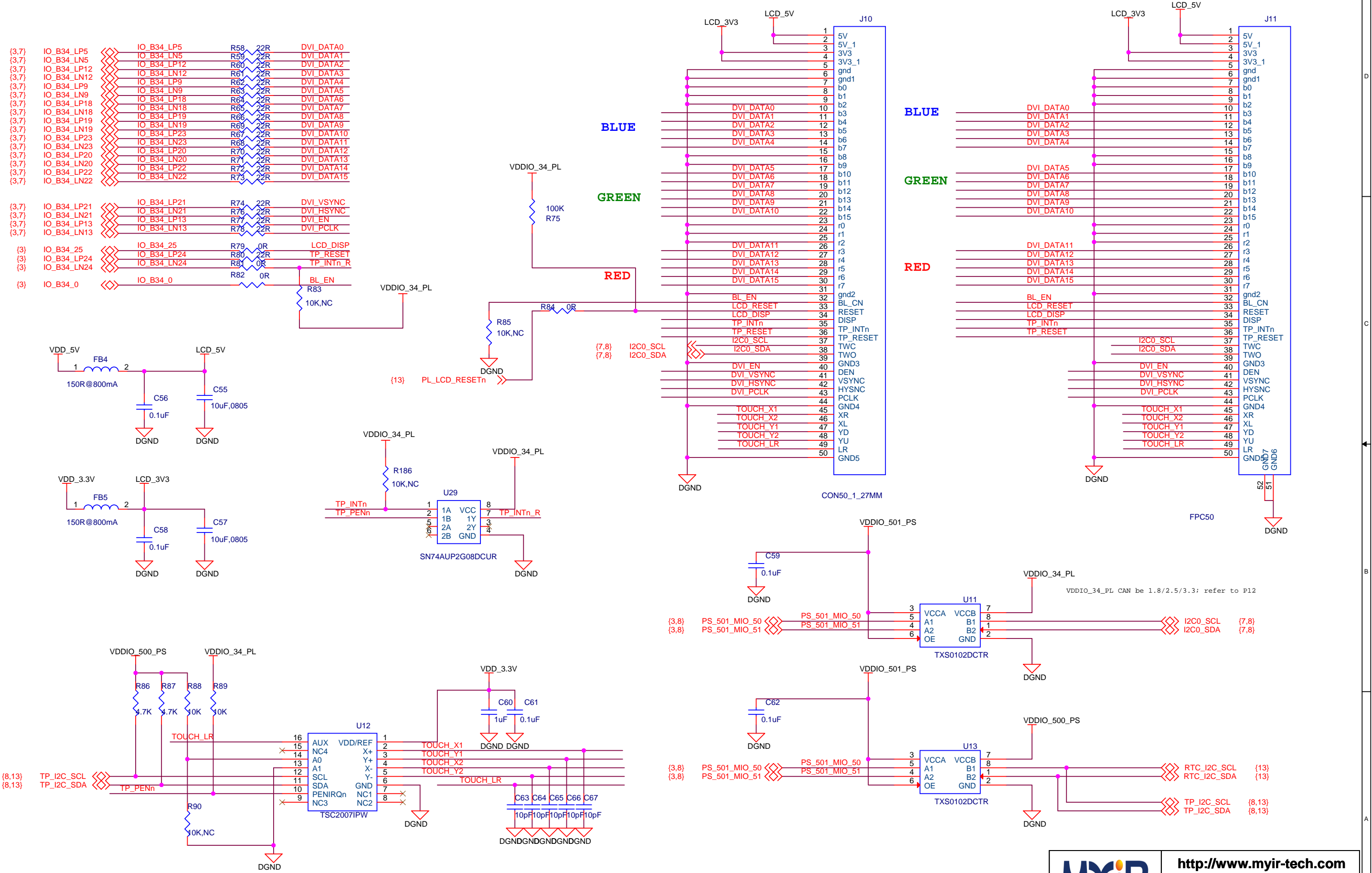


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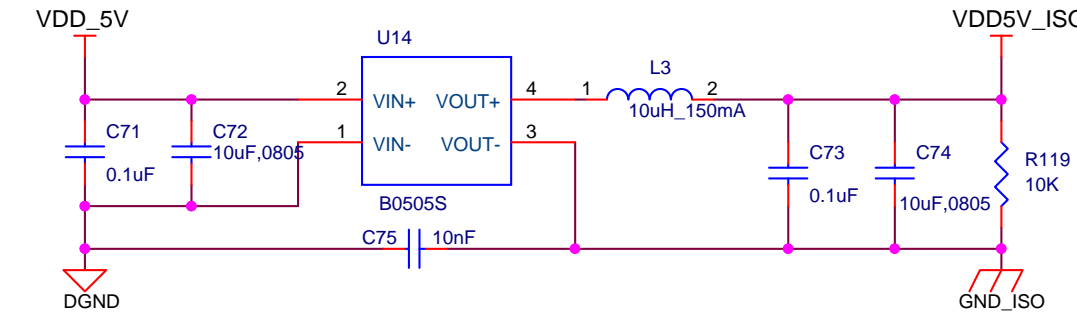
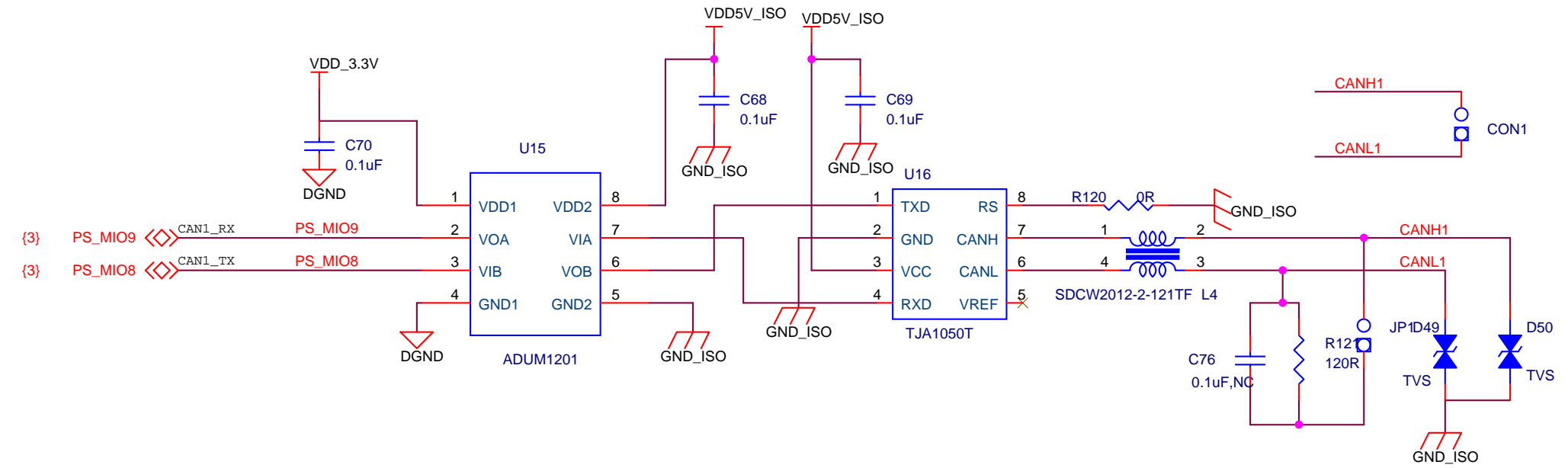
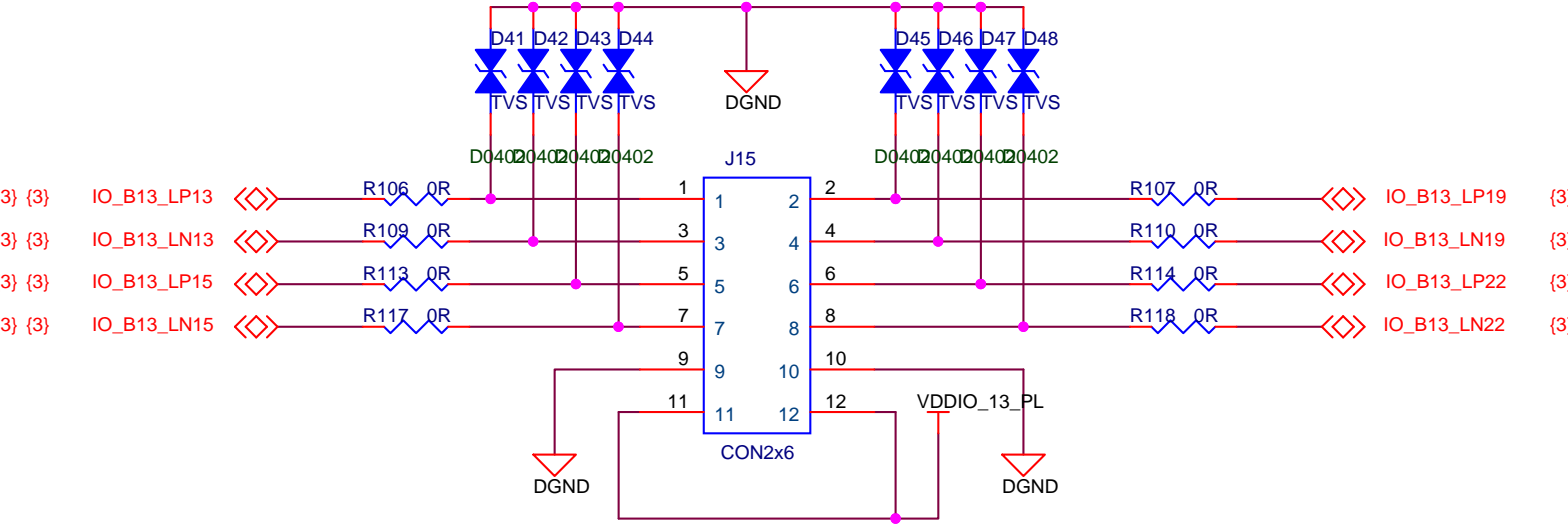
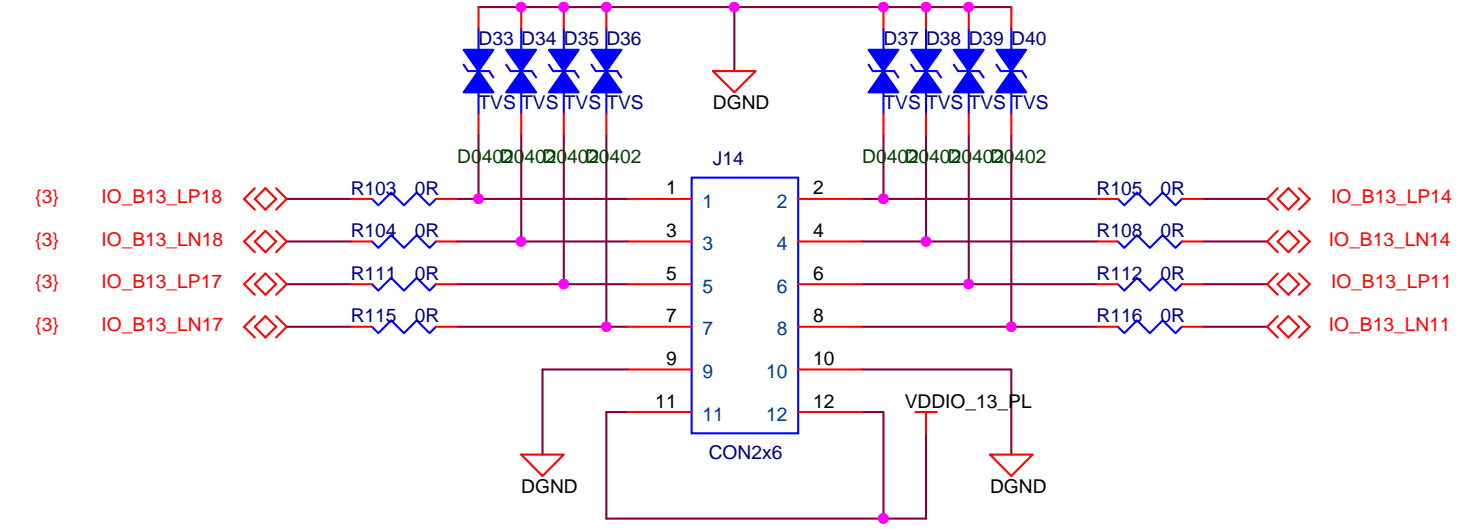
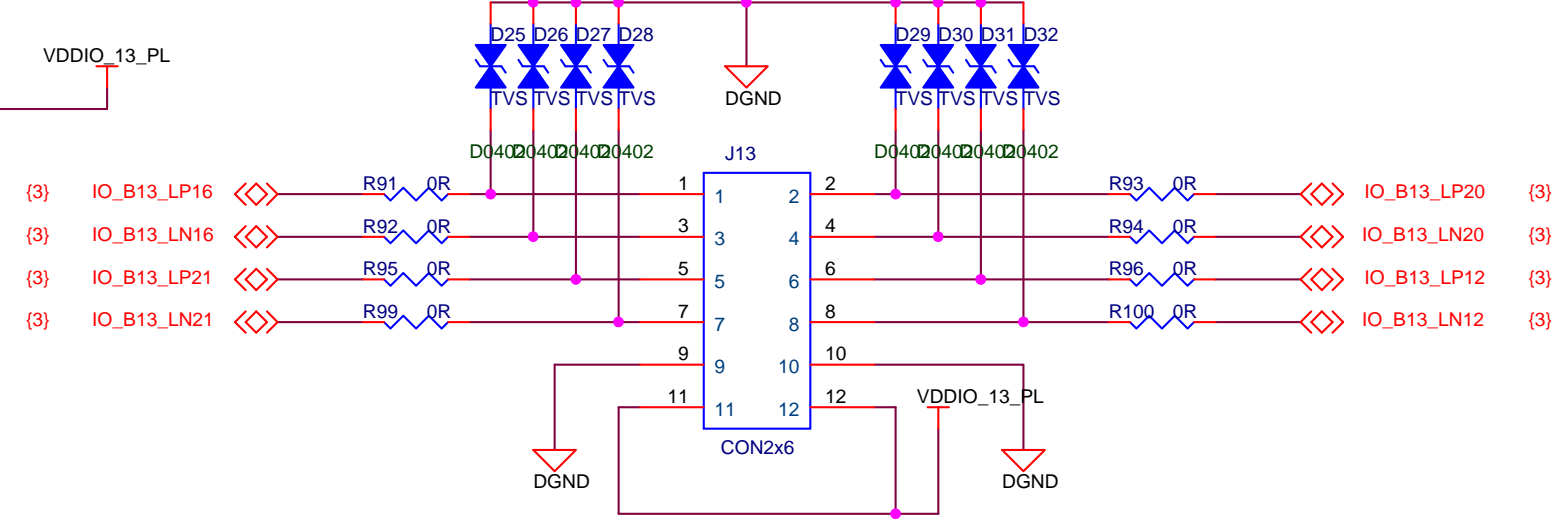
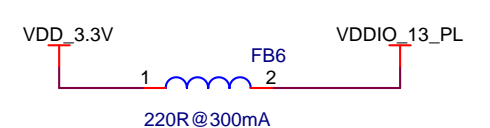
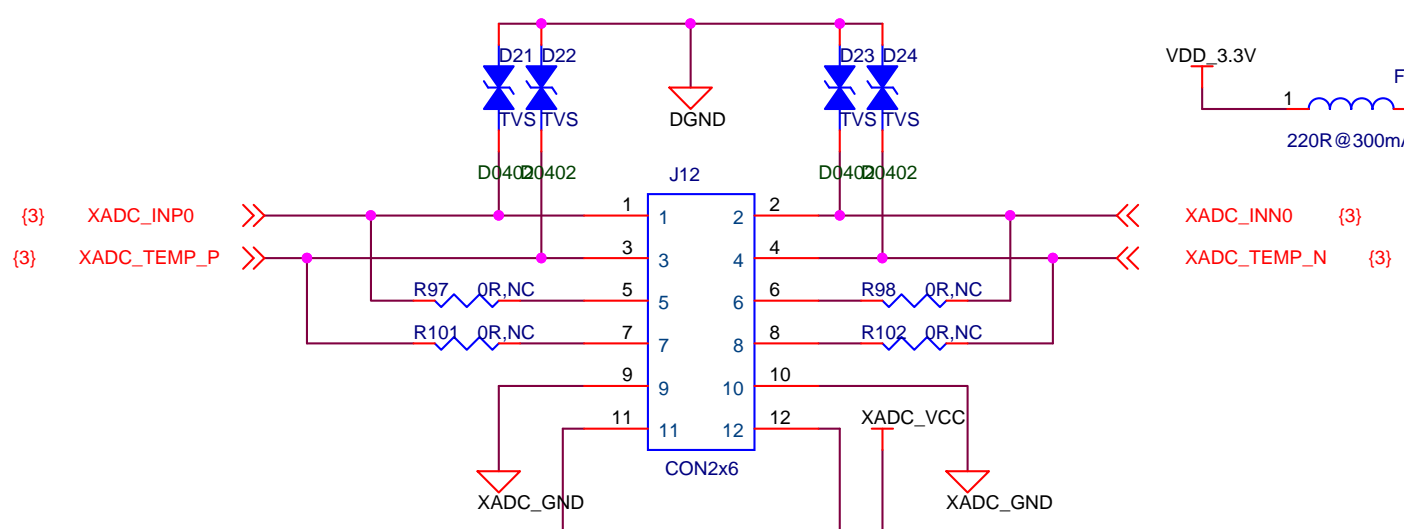




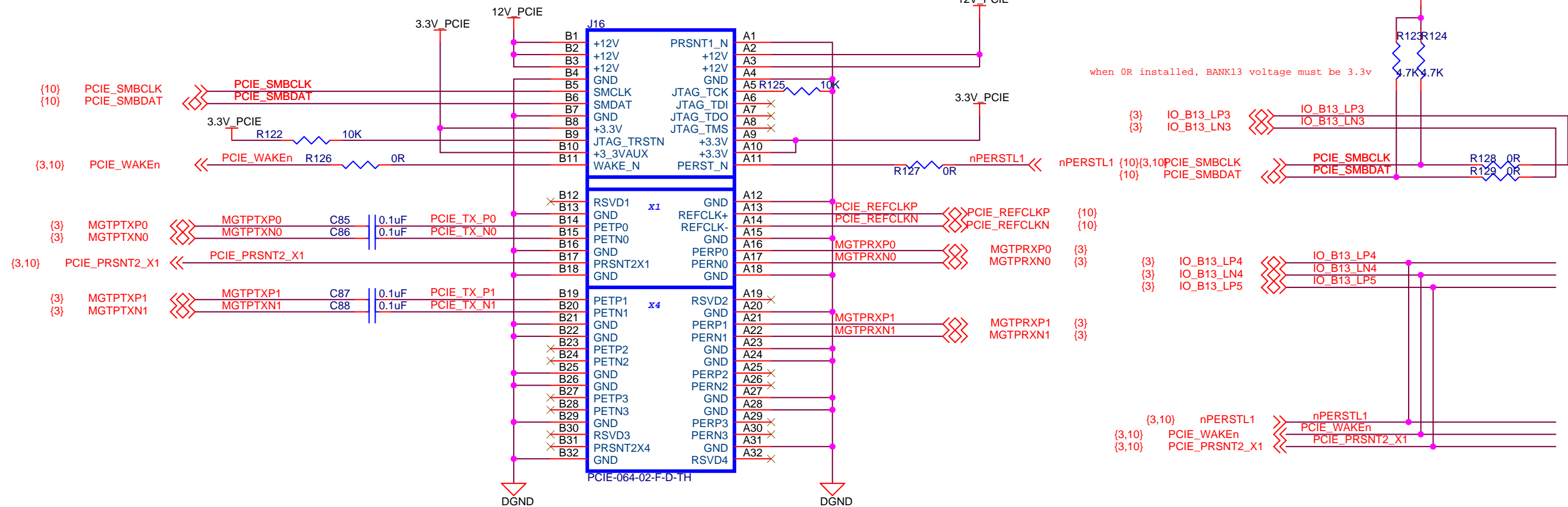
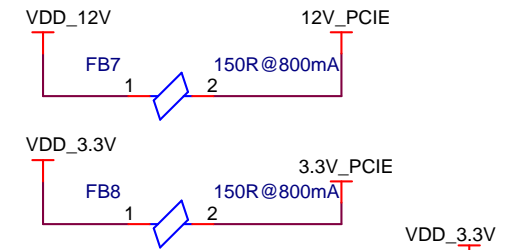
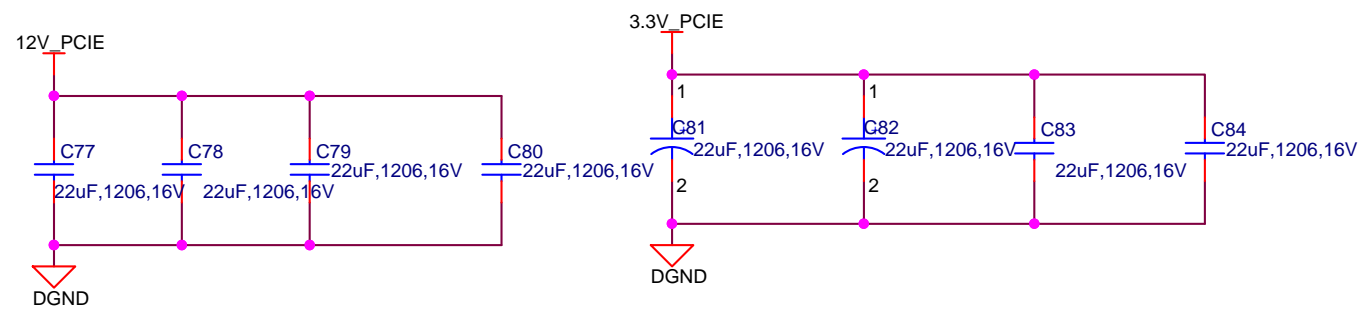




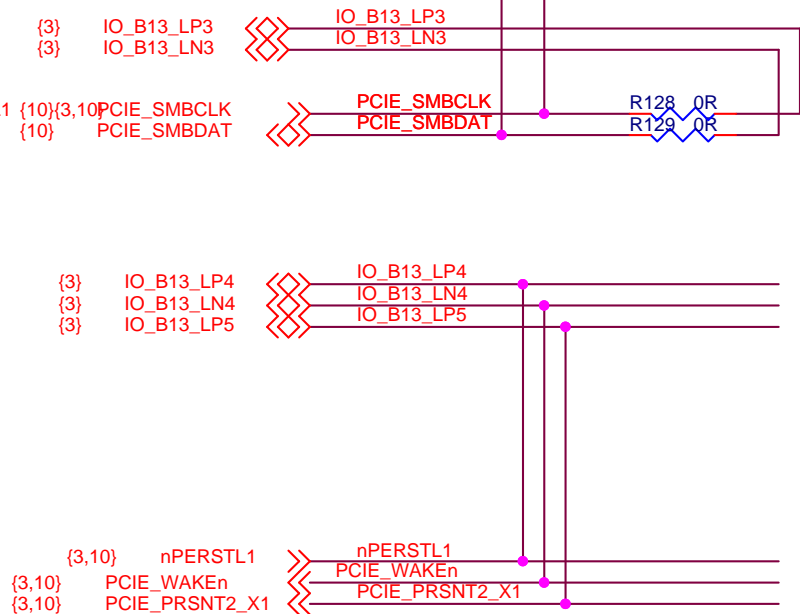
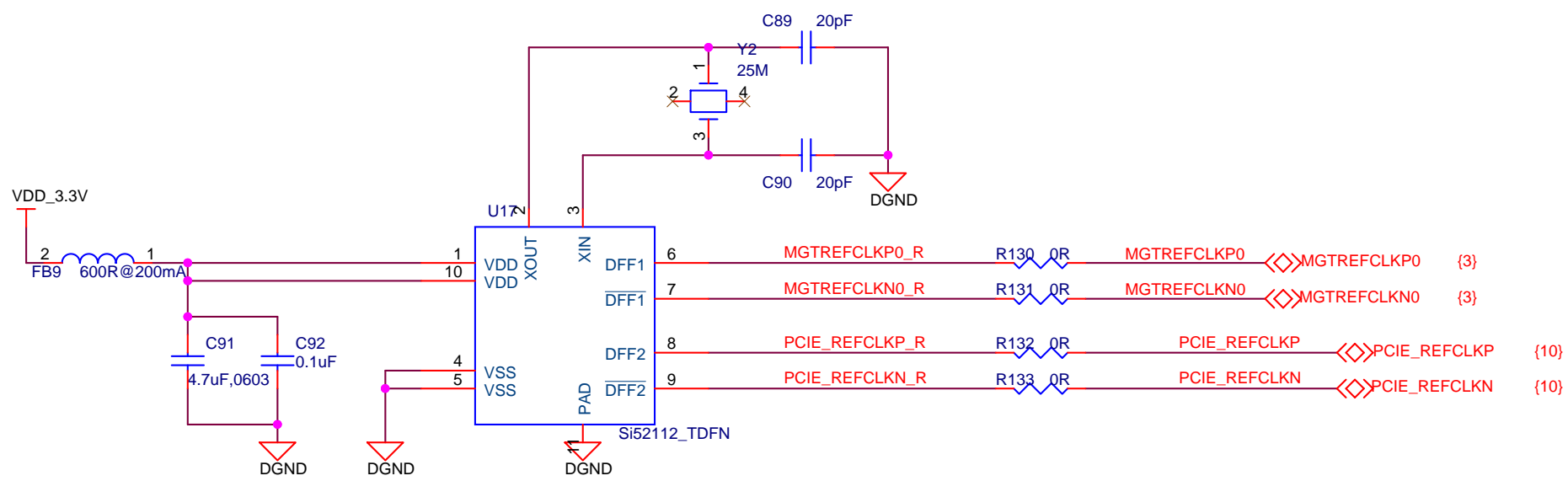




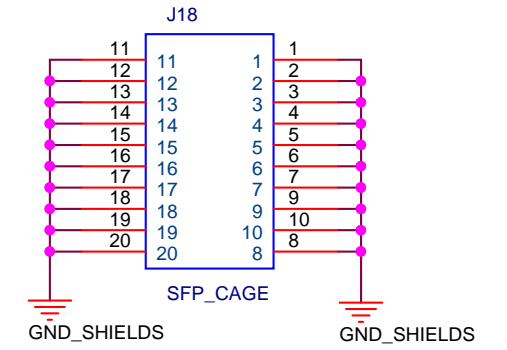
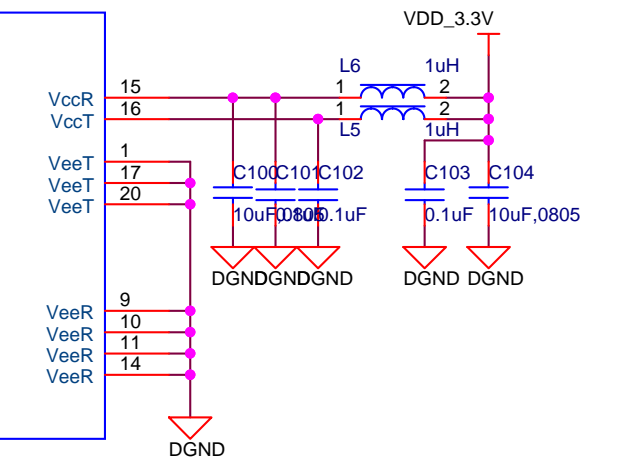
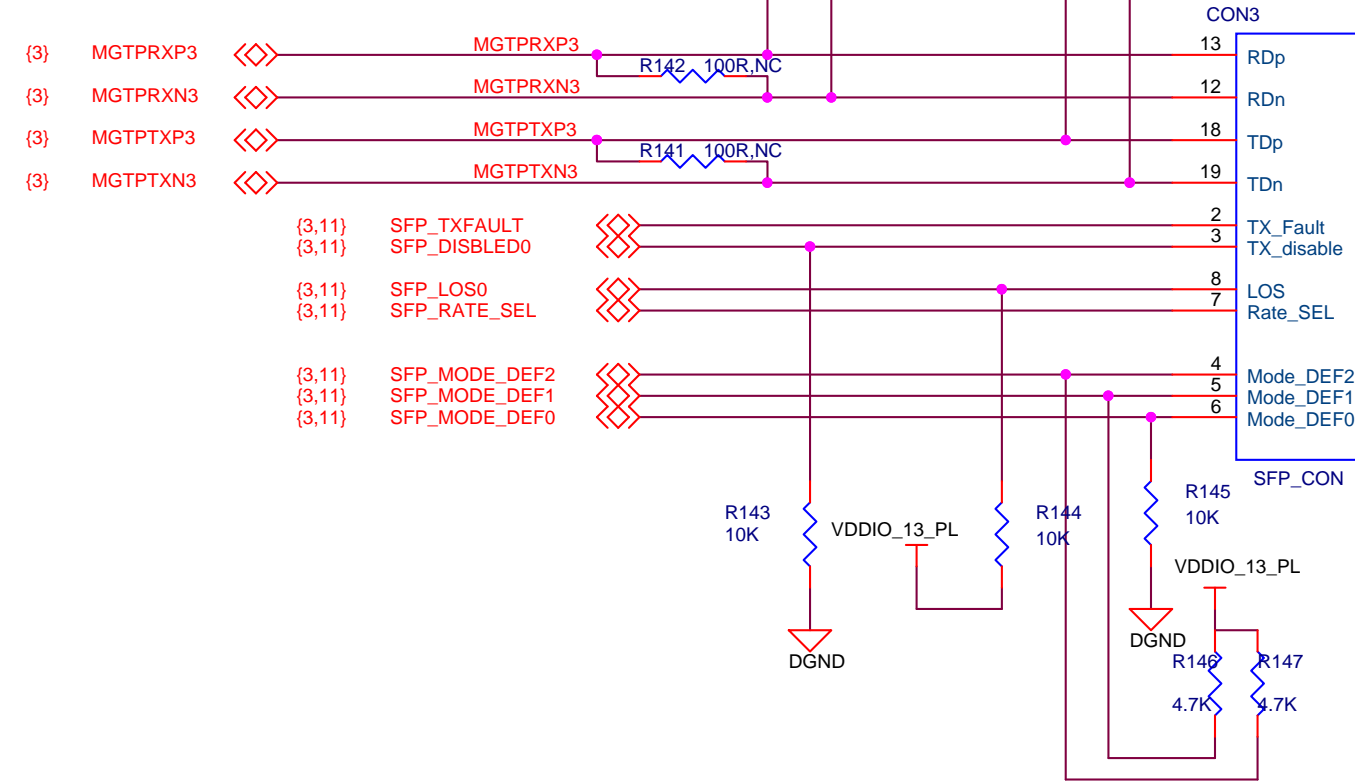
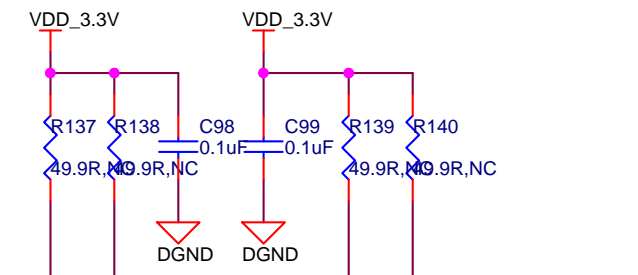
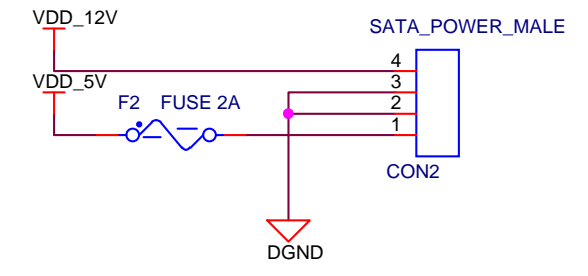
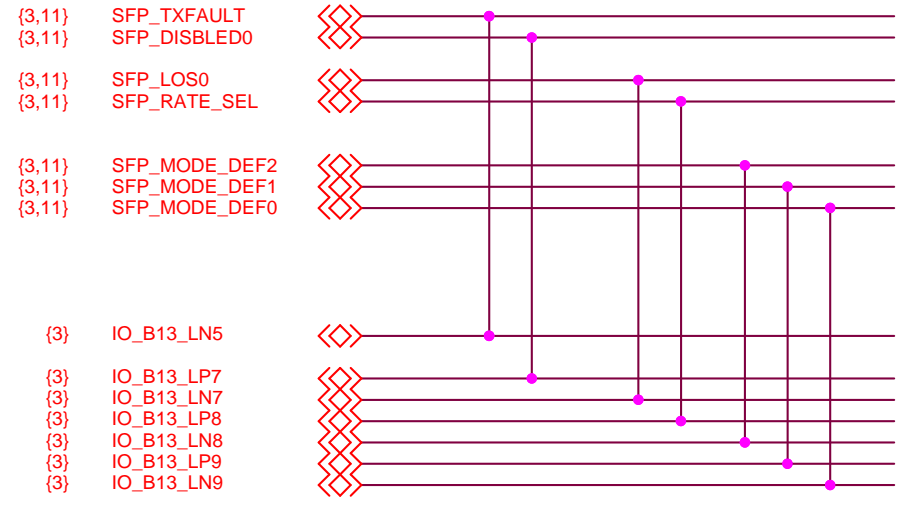
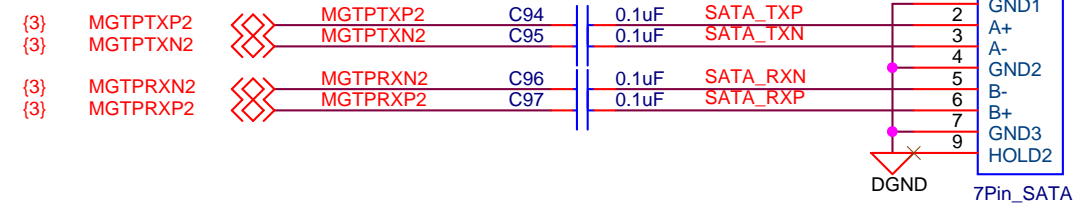
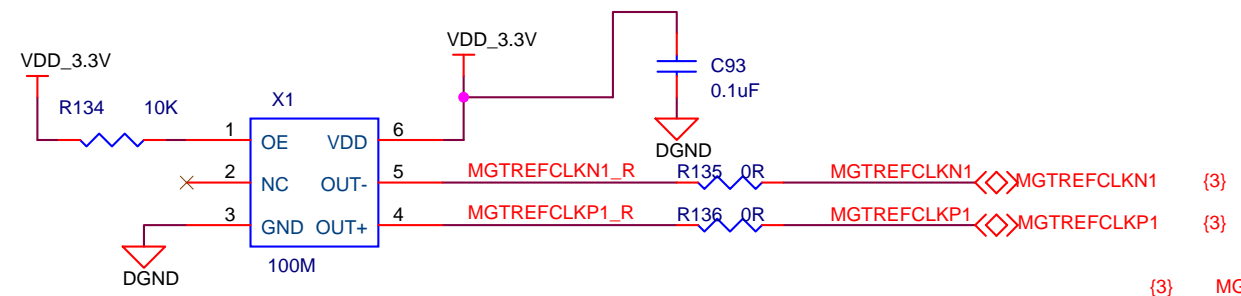
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Draw By: MYIR	Date: Thursday, July 13, 2017	Sheet: 9 of 13	



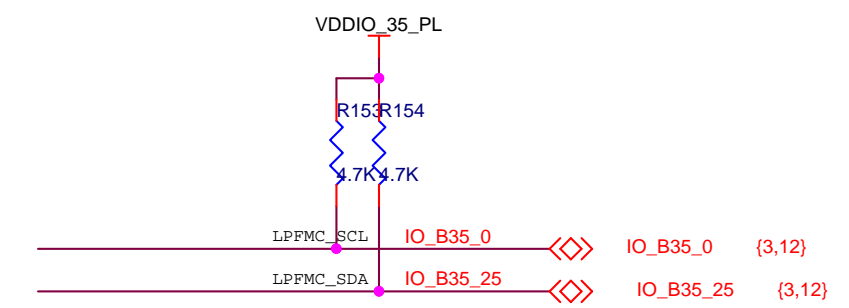
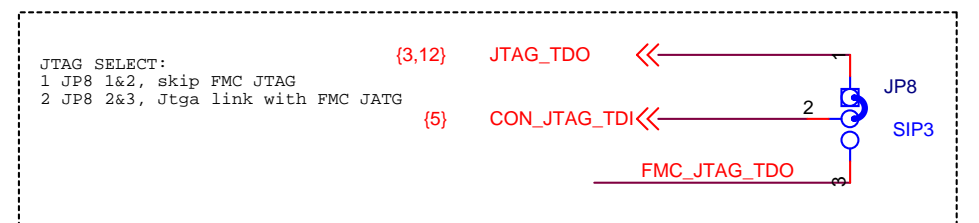
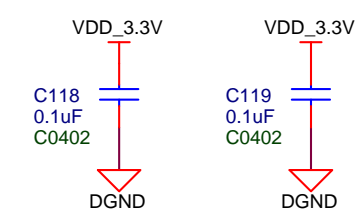
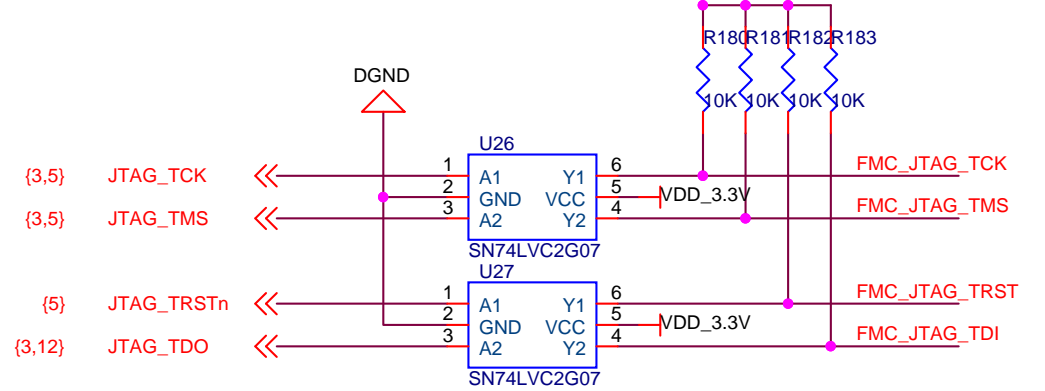
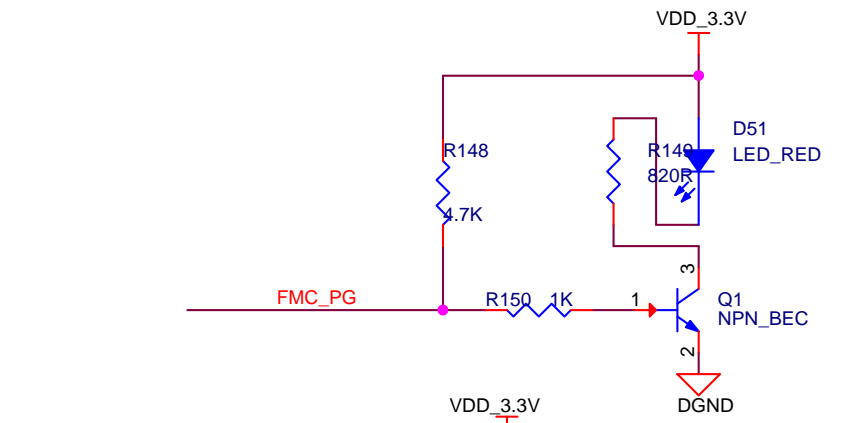
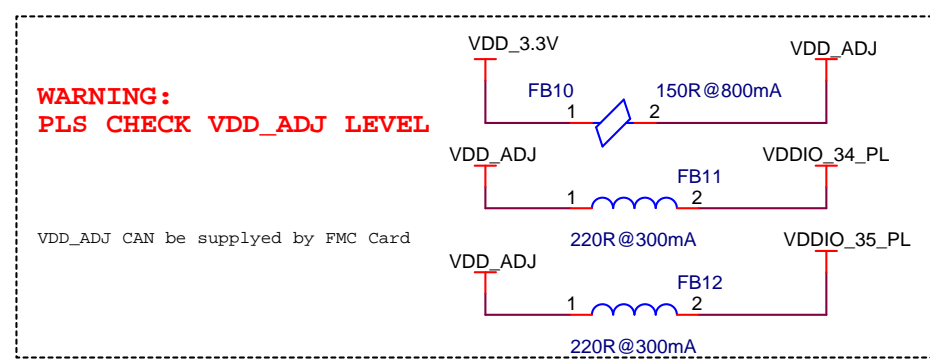
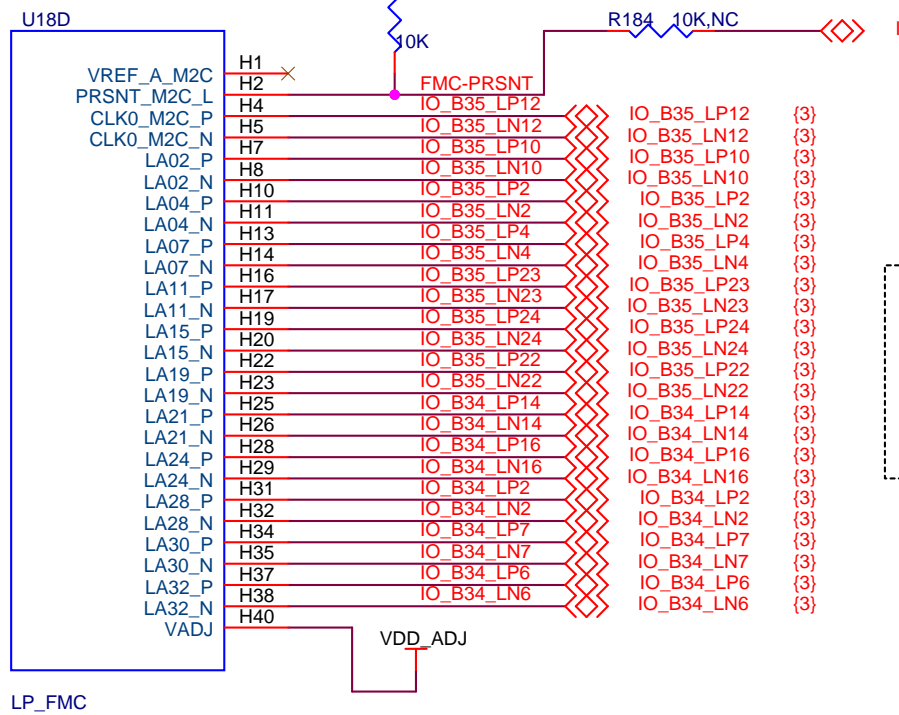
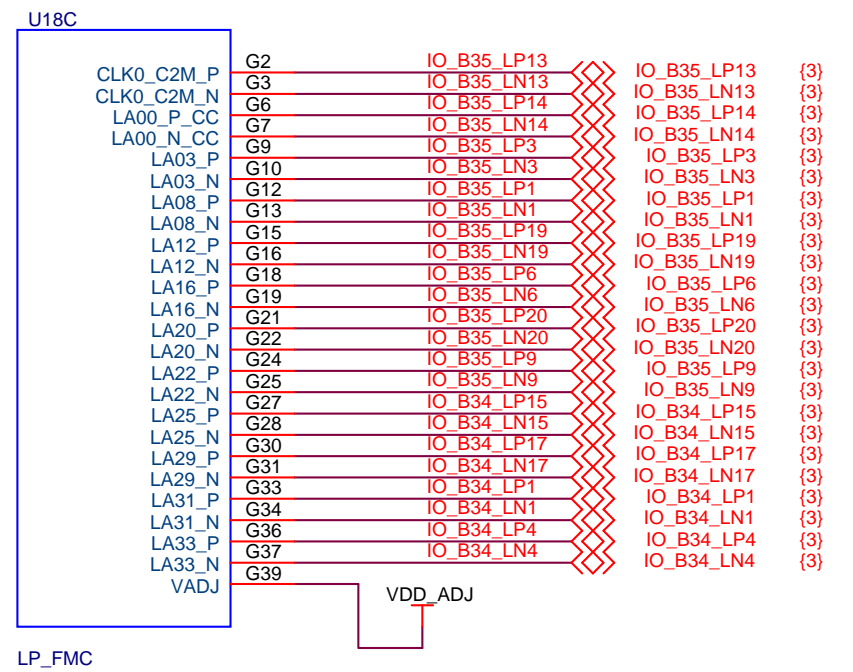
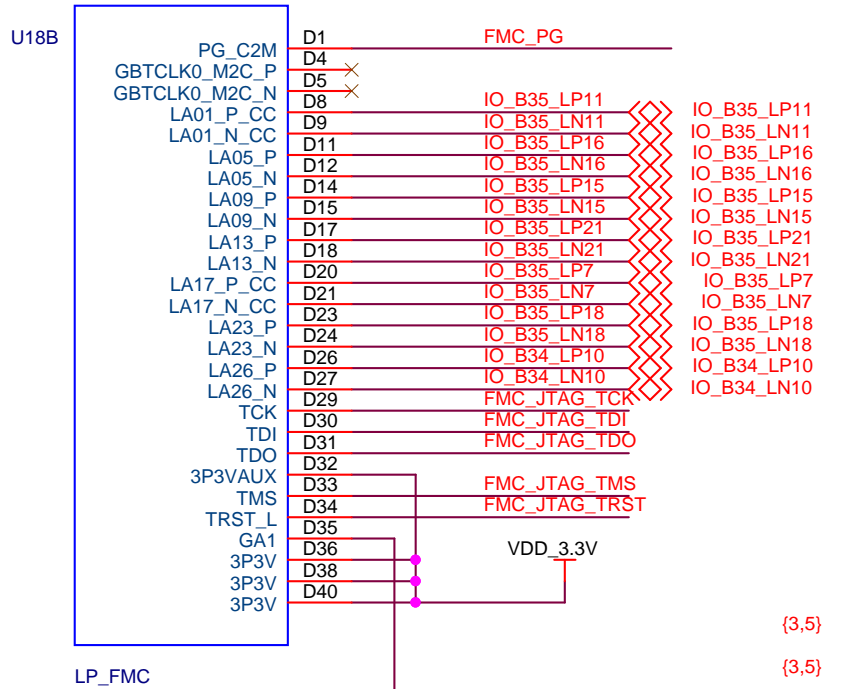
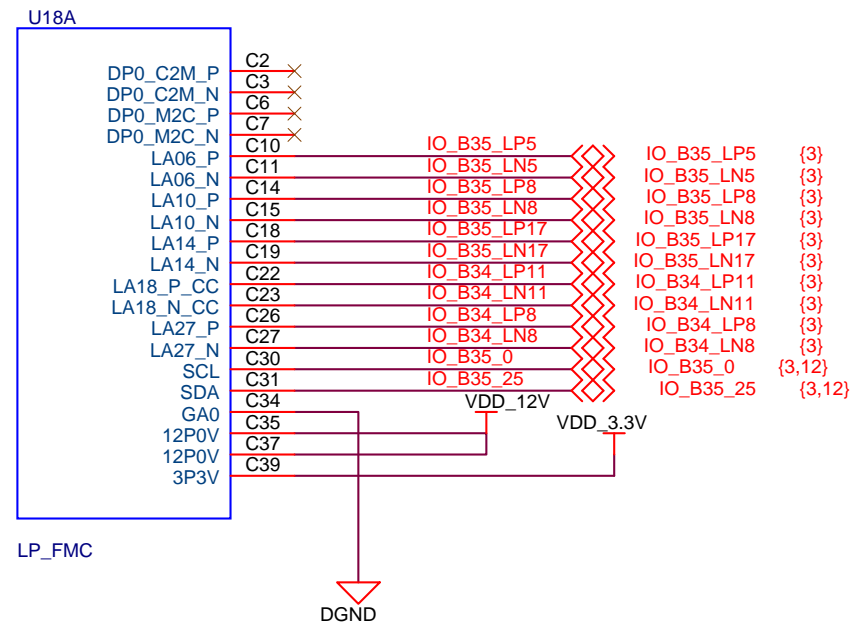
when 0R installed, BANK13 voltage must be 3.3v



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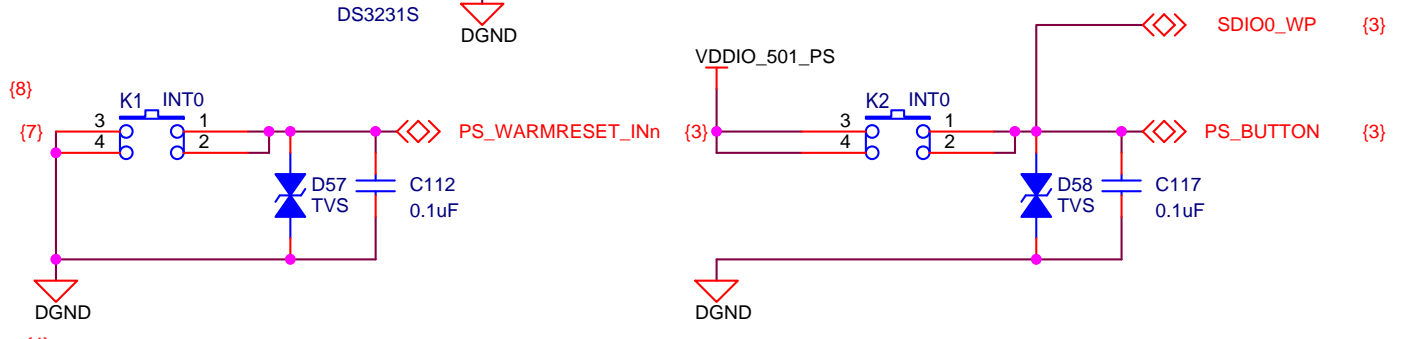
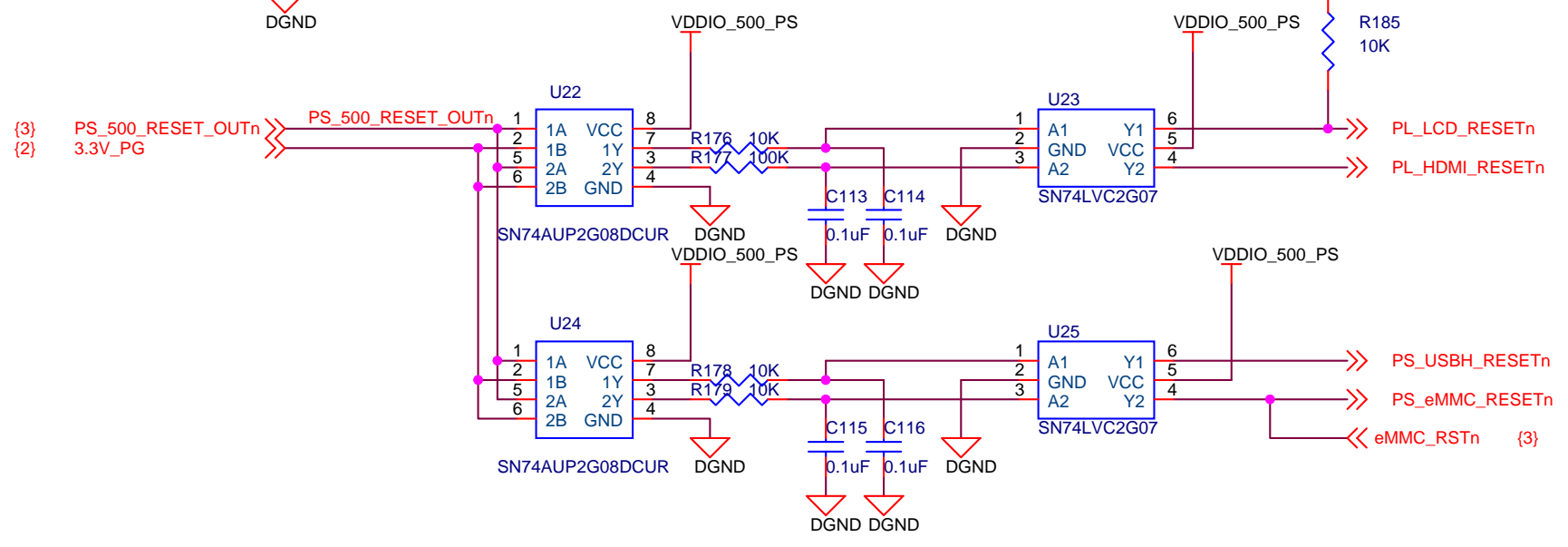
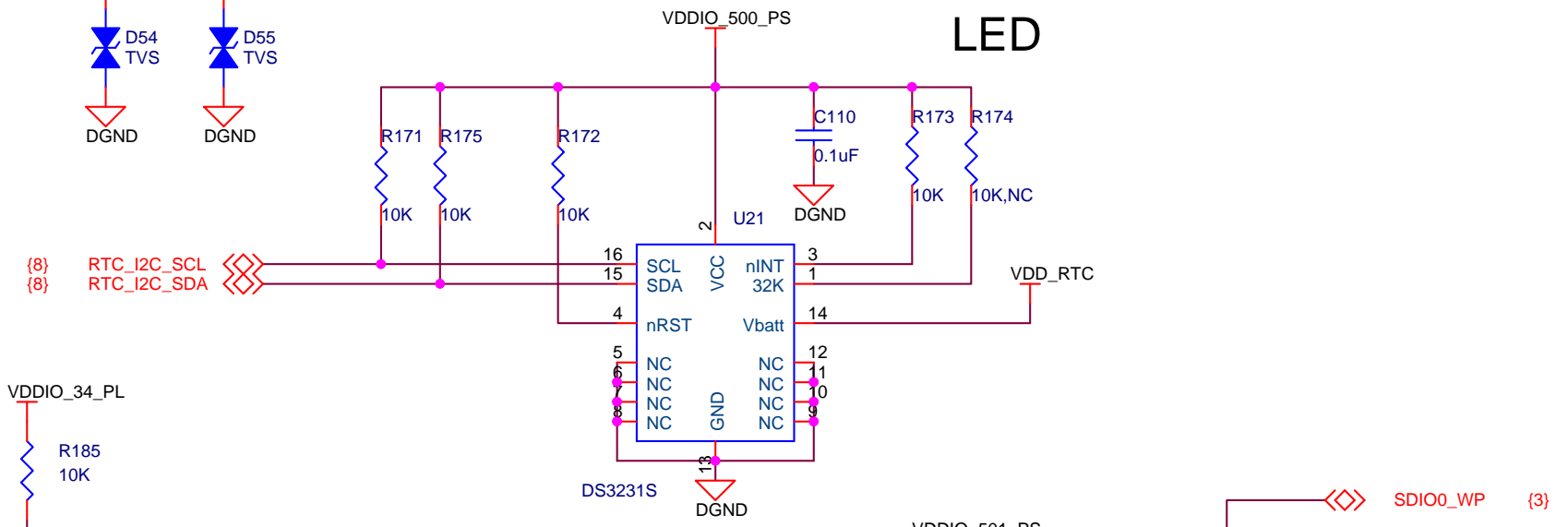
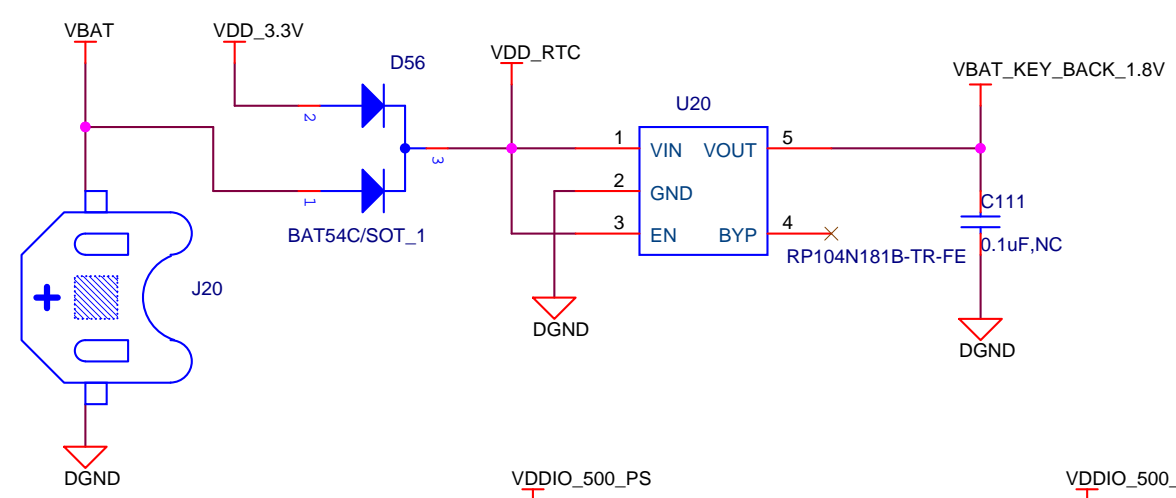
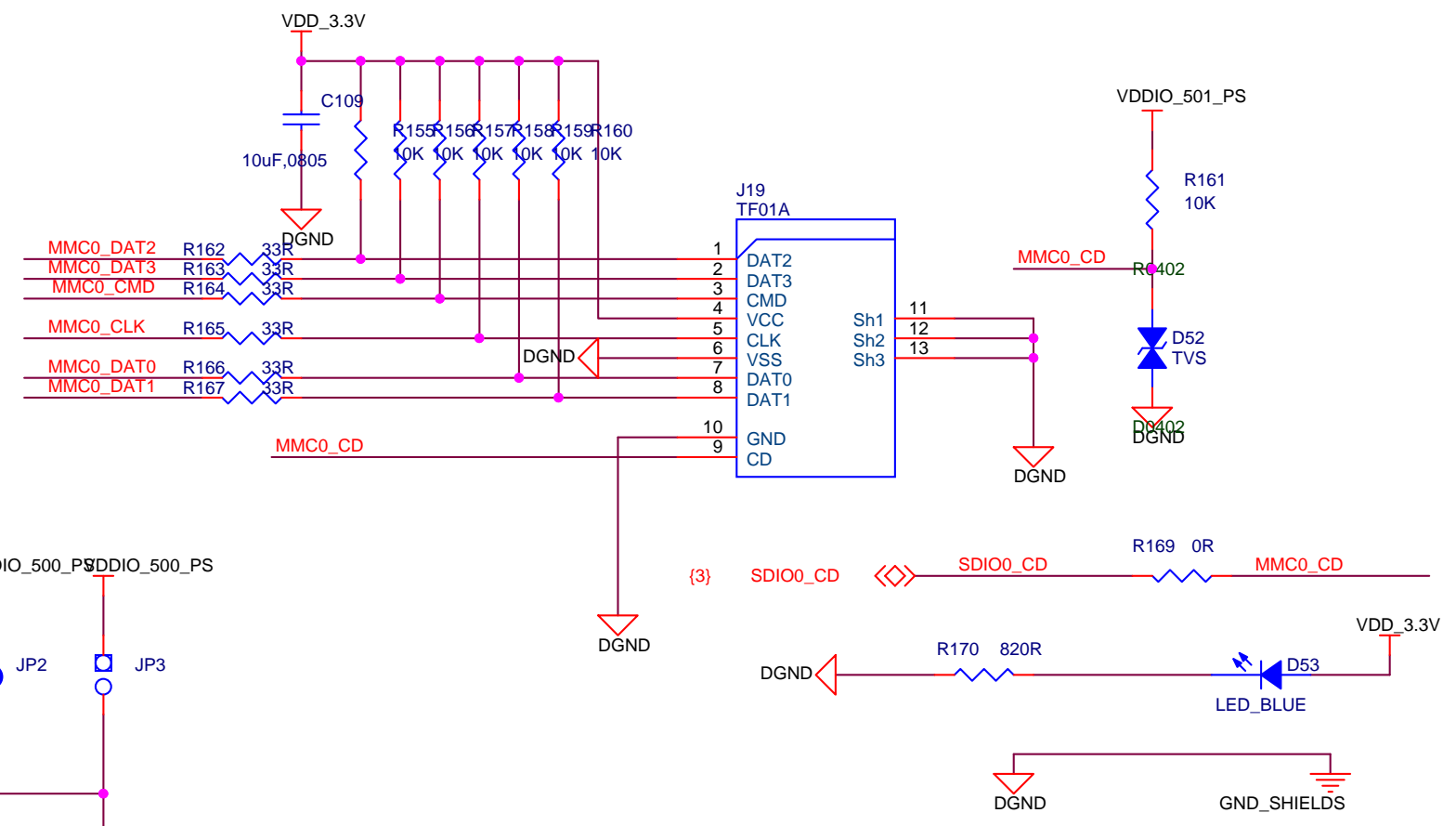
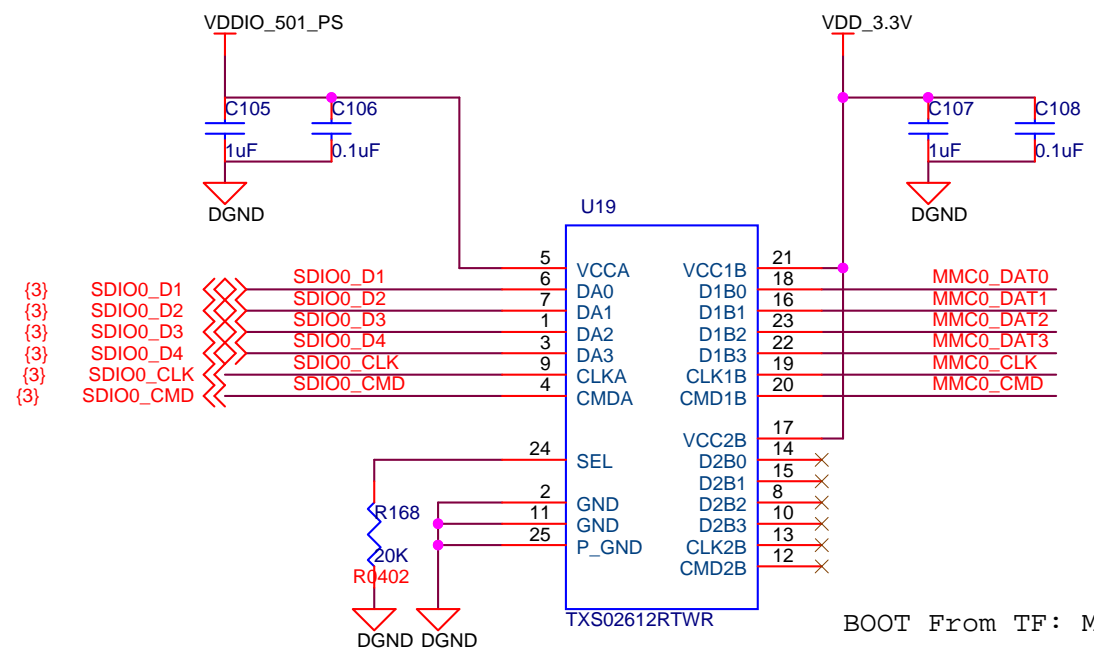
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Title: MYB-ZYNQ7Z010\_20-SCH

Size: B	Document Number: P12_LPFMC	Rev: VER 1
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Draw By: MYIR	Date: Thursday, July 13, 2017	Sheet: 13 of 13	